High-Performance Planar Inductor on Thick Oxidized Porous Silicon (OPS) Substrate

Choong-Mo Nam and Young-Se Kwon

***Abstract*— To obtain a high-performance planar inductor, we used the oxidized porous silicon (OPS) layer with 25-μm-thick SiO_2 as substrate. The measured radio frequency (RF) performances of the planar inductor on the OPS layer are comparable to those on the semi-insulating GaAs substrate.**

For a 6.29-nH inductor, resonant frequency of 13.8 GHz and maximum quality factor (Q) of 13.3 are obtained. These results show that the utilization of the OPS layer can push silicon passive monolithic microwave integrated circuit (MMIC) technology at least up to 12 GHz.

***Index Terms*— MMIC, oxidized porous silicon (OPS), planar inductor.**

I. Introduction

PLANAR inductors have been implemented in practical systems such as low-noise amplifiers, mixers, power amplifiers, and voltage-controlled oscillators. Usually, the planar inductors are on either GaAs or silicon substrate. For GaAs substrate, semi-insulating substrate can be assured and high-performance microwave devices can be fabricated. Unfortunately, GaAs is expensive, fragile, and has low thermal conductivity. On the other hand, silicon has the advantages of low cost and high thermal conductivity.

Actually, the modern silicon IC process offers good active devices that have high f_T and $f_{\max}$ [1]. However, it is difficult to realize high Q inductors on silicon substrate because of the semiconducting nature of silicon and limited metal thickness [2], [3]. To obtain high-performance inductors, many approaches using high-resistive silicon with micro-machining technique [4], glass layer [5], thick polyimide layer [6], and multilevel interconnection in silicon substrate [7]–[9] have been reported.

In this letter, we propose a thick OPS layer on silicon as a substrate for a high-performance planar inductor as shown in Fig. 1, and the performance of the fabricated inductor on OPS layer is presented. The performances of the fabricated thin-film resistor and MIM capacitor will be reported elsewhere.

Instead of direct oxidation of bulk silicon, short-time (less than an hour) oxidation process of porous silicon was utilized to make the thick oxide layer. It was possible to make a thick oxide layer thicker than 30 μm, because the oxidation of porous silicon was performed by the reaction of side wall of pores. Thus, the process of OPS layer formation has lower cost and lower process time than the other chemical vapor deposition (CVD) methods. Because of this thick oxide layer, the semiconducting nature of silicon will not have a detrimental effect on the quality of the fabricated planar inductor.

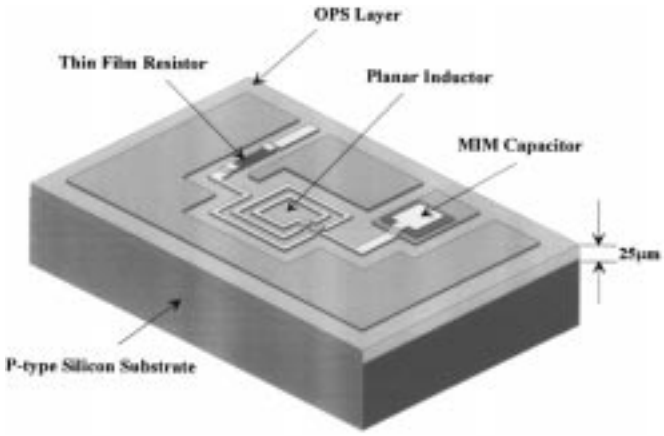

Fig. 1. Illustration of OPS layer on silicon substrate. The microwave passive elements such as planar inductor, thin-film resistor, MIM capacitor, and coplanar waveguide are fabricated on OPS layer. The thickness of the OPS layer is dependent on porous silicon layer thickness, which is determined by anodization conditions such as anodic reaction time and anodic current density.

II. Experimental

The OPS layer is obtained by anodization and oxidation process in silicon substrate. Porous layers were prepared on (100) B-doped silicon substrates of 5–7 Ω-cm resistivity by anodization process [10]. Anodization of p-type silicon was carried out under the condition of 30 mA/cm^2 in electrolyte solution of HF(48 w/o): $C_2H_5OH = 1:1$. The experiments were conducted at room temperature ($\sim$22 °C). In order to obtain an uniform-thickness-porous silicon, aluminum films were formed on the back of the wafers by vacuum evaporation. The growth rate of porous silicon layer was 1.4 μm/min in the anodic current density of 30 mA/cm^2.

The porous silicon layer was preoxidized at 350 °C under dry oxygen of atmospheric pressure for 30 min. This preoxidation step only creates a thin layer of silicon dioxide all over the pore walls which prevents pore reorganization during further heat treatment [11]. The preoxidized wafer was oxidized for 5 min in wet oxygen in the temperature range of 1110–1120 °C.

Planar inductors on OPS layer with 25-μm-thick SiO_2 were fabricated by photolithography, vacuum evaporation of Ti/Au layers (first metal), and 2.3-μm-thick Au plating (second

Manuscript received February 27, 1997.

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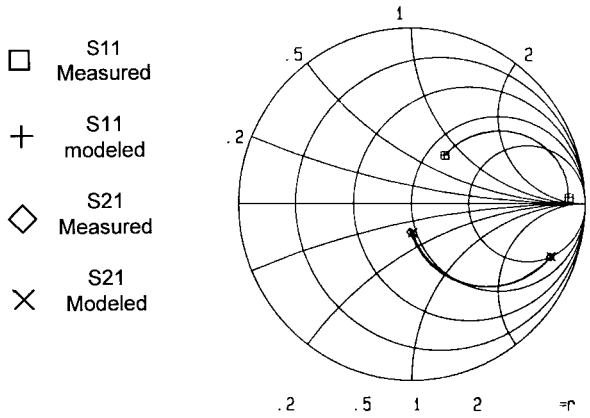
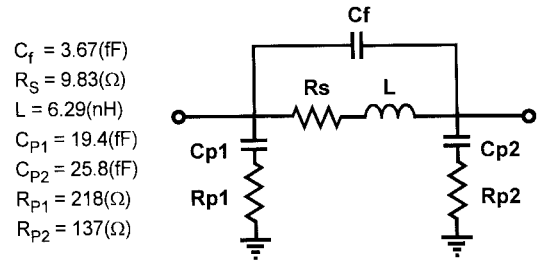
Publisher Item Identifier S 1051-8207(97)05412-3.

TABLE I
COMPARISON OF DIFFERENT IMPLEMENTATIONS OF SPIRAL INDUCTORS ON SILICON SUBSTRATE. THE PLANAR INDUCTOR WITH HIGH RESONANT FREQUENCY AND HIGH QUALITY FACTOR ARE FABRICATED BY USING THICK OPS LAYER AND AU METALLIZATION

L (nH)	No. of turns	W/S (μm/ μm)	Self-resonant frequency(GHz)	Qmax (f[GHz])	Fabrication technology	Ref.
9.70	9	6.5/5.5	2.47	3(0.9)	1.7 μm SiO_2 layer	[2]
6.0	6.5	15/5	4.4	3(1.2)	1.7 μm SiO_2 layer	[3]
9.33	6	7/13	6.0	5.6(1.3)	9μm-thick polyimide layer	[6]
5.10	6	12/4	10.3	11.5(1.8)	multi-level interconnect	[8]
6.29	4.5	5/5	13.8	13.3(4.6)	25μm-thick OPS layer	this work



(a)



(b)

Fig. 2. (a) The modeled and the measured S-parameters of the 6.29-nH inductor which was fabricated on OPS layer with 25-μm-thick SiO_2. The measured frequency range is from 1 to 12 GHz and (b) an equivalent circuit of the spiral inductor on OPS layer. The equivalent circuit parameters and the modeled S-parameters are extracted by EEsof Libra simulator.

metal). Metal stripe width (W) was 5 μm and the spacing (S) between the metal stripes was 5 μm. The number of turns (N) and the size of inner area (D) were 4.5 and 140 $\times$ 140 μm^2, respectively.

III. RESULTS AND DISCUSSION

The frequency-dependent S-parameters of the inductor on OPS layer were measured by vector network analyzer and Cascade-on-wafer-probe up to 12 GHz and the parasitics were de-embedded using dummy patterns. Fig. 2 shows the modeled and the measured S-parameters of 4.5-turn inductor.

The inductor had an inductance value of 6.29 nH and an estimated resonant frequency of 13.8 GHz. These values were calculated from the modeled S-parameters using EEsof Libra simulator.

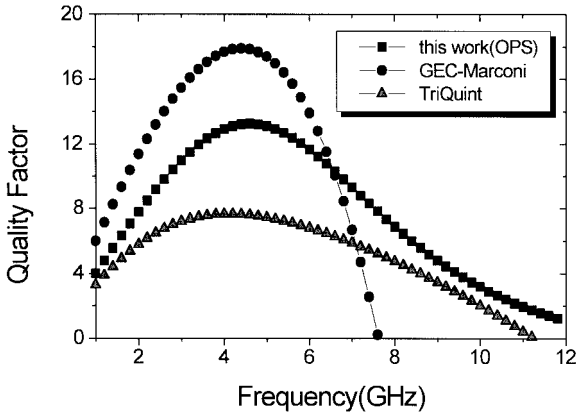


Fig. 3. Comparison of quality factors of inductors as a function of frequency. The inductance values of GEC-Marconi and TriQuint inductor are 5.86 and 5.92 nH, respectively. These data are from GEC-Marconi's and TriQuint's GaAs MMIC data sheet.

The value of the quality factor (Q) is given by

$$Q = \frac{\mathrm{Im}\,[Z_{in}]}{\mathrm{Re}\,[Z_{in}]} \tag{1}$$

where $\mathrm{Re}\,[Z_{in}]$ is the real part of the input impedance of spiral inductor and $\mathrm{Im}\,[Z_{in}]$ is the imaginary part of the input impedance of spiral inductor.

In Fig. 3, the quality factor of the inductor fabricated on OPS layer is compared with that of GEC-Marconi inductor which uses 9-μm-thick polyimide layer on GaAs substrate and that of the airbridge inductor on the semi-insulating GaAs substrate produced by TriQuint. The quality factor of the inductor on OPS layer is comparable to that of GEC-Marconi inductor but is slightly better than that of TriQuint inductor.

This result indicates that a thick oxide layer increases the resonant frequency and the quality factor in planar inductor because of the reduced parasitic resistance and low parasitic capacitance between inductor metal and the silicon substrate.

The performances of several inductors fabricated on silicon substrates are shown in Table I. The high Q inductance was obtained which is large enough for radio frequency (RF) choke and matching element. Thus, the fabrication process of OPS layer on silicon can push silicon passive MMIC technology at least up to 12 GHz.

IV. CONCLUSION

In summary, planar inductors with high resonant frequency and high Q are fabricated on OPS substrate with 25-μm-thick

SiO_2. The measured RF performances of the planar inductor on OPS layer are very comparable to those on the semi-insulating GaAs substrate.

As matching or biasing elements, the planar inductors on OPS layer can be used in applications such as 900-MHz communications and several gigahertz-range satellite reception, including GPS and DBS.

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